Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Original): A method of representing a numerical value in an information processing apparatus comprising:

    a. storing an integer portion of said numerical value in a first storage area;

    b. storing a fractional portion of said numerical value in a second storage area;

    c. wherein said first storage area and said second storage area are non-contiguous;

    d. wherein an integer portion of said numerical value can be fully determined by reference to said first storage area; and

    e. wherein a fractional portion of said numerical value can be fully determined by reference to said second storage area.

2. (Original): The method according to claim 1 wherein said integer portion is stored in said first storage area according to a standard binary integer format.

3. (Original): The method according to claim 2 wherein said integer portion is stored in said first storage area as a signed 2's complement binary integer.

4. (Original): The method according to claim 1 wherein said fractional portion is stored in said second storage area according to a standard binary integer format.

5. (Original): The method according to claim 4 wherein said fractional portion is multiplied by a scale value and then stored in said second storage area according to a standard binary integer format.

6. (Original): The method according to claim 5 wherein said scale value is an integer power of 10.

7. (Original): The method according to claim 4 wherein said fractional portion is stored in said second storage area as a signed 2's complement binary integer.

8. (Original): The method according to claim 1 wherein:

    said integer portion is stored with a separate integer portion sign bit; and

    said fractional portion is stored with a separate fractional portion sign bit.

9. (Original): The method according to claim 1 further comprising:

determining character codes for said numerical value by separately determining character codes for said integer portion and said fractional portion; and

concatenating separately determined character codes to provide character codes for said numerical value.

10. (Original): An apparatus in a computing system for handling real numbers comprising logic modules to perform the method as recited in claim 1.

11. (Amended): A method allowing an information handling system to handle a range of real numbers comprising:

creating an IP.FP data template in a memory of said information handling system;

wherein said data template provides non-contiguous storage areas for:

a ~~decimal~~ an integer part, and

a fractional part of real number values;

using a plurality of IP.FP logic routines for performing numerical and logic operations on numerical values stored in IP.FP format.

12. (Original): A method of speeding up operation of a computer system performing math operations on numerical values comprising:

a. storing an integer portion of a numerical value in a first storage area;

b. storing a fractional portion of said numerical value in a second storage area;

c. wherein said first storage area and said second storage area are non-contiguous;

d. using a plurality of custom functions to perform logic and arithmetic operations on said numerical value, said custom functions explicitly handling carry and bit shifting operations involving said numerical value.

13. (Original): A device for handling numerical values in an information processing system comprising:

a. first means for storing integer portions of said numerical values;

b. second means for storing fractional portions of said numerical values;

c. said first means and said second means being non-contiguous;

d. wherein an integer portion of a numerical value can be fully determined from said first means; and

e. wherein a fractional portion of a numerical value can be fully determined from said second means.

14. (Original): The device of claim 13 further wherein:

an integer portion is stored in said first means using a standard binary integer format; and

said integer portion is stored in said first means as a signed 2's complement binary integer.

15. (Original): The device of claim 13 further wherein:

a fractional portion is multiplied by a scale value and then stored in said second means using a standard binary integer format.

16. (Original): The device of claim 13 further wherein:

said integer portion is stored with a separate integer portion sign bit; and

said fractional portion is stored with a separate fractional portion sign bit.

17. (Original): The device of claim 13 further comprising:

means for determining character codes for a numerical value stored as an integer portion and an fractional portion that separately determine character codes for said integer portion and said fractional portion.

18. (Original): A fixed media containing logical instructions that when loaded into an appropriately configured digital apparatus causes the apparatus to operate in accordance with the method of claim 1.

19. (Original): A system of improving performance in handling numerical value in an information processing apparatus comprising:

a first logic routine for analyzing numerical values in said information processing system, said first logic routine:

storing an integer portion of said numerical value in a first storage area;

storing a fractional portion of said numerical value in a second storage area; and

returning a pointer to said first and said second storage area;

a numerical processor module comprising:

a logic interface for receiving pointers to one or more numerical values stored as integer portions and fractional protions;

a logic interface for receiving an indication of a requested operation to be performed on said one or more numerical values;

processing logic for performing said requested operation and for explicitly handling any necessary carry or bit-shifting operations of said numerical values.

20. (Original): The system of claim 19 wherein said system is implemented as run-time computer logic instructions executing in an application and/or operating system process space of an information processing system.

21. (Original):   The system of claim 19 wherein said system is implemented comprising one or more custom logic hardware components of an information processing system.